UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,651	04/18/2001	Robert Warren Sherburne, Jr		9125

38236 7590 09/16/2004

DOMINIK J. SCHMIDT
P.O. BOX 20541
STANDFORD, CA 94309

EXAMINER	
BUTLER, DENNIS	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,651	SHERBURNE, JR, ROBERT WARREN	
	Examiner	Art Unit	
	Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the amendment received on June 8, 2004. Claims 1-20 are pending.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. The terminal disclaimer filed on June 8, 2004 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of copending Application No. 09/814,355 has been reviewed and is NOT accepted.

The terminal disclaimer does not comply with 37 CFR 1.321(b) and/or (c) because:

> The disclaimer fee in accordance with 37 CFR 1.20(d) has not been submitted, nor is there any authorization in the application file to charge a specified Deposit Account or credit card.

4. Claims 1-3, 6, 9 and 19-20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 and 6 of copending Application No. 09/814,355. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are directed to substantially the same invention including one or more processing units and a controller varying the clock frequency to each processing unit. Although claims 1-3 and 6 of the present application do not recite the processor including a memory, it is well known that processors routinely include memory units. In addition, claims 19 and 20 of the present application recite the processor including a buffer memory.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

5. Claims 8 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 8, the phrase "the plurality of clocks" lacks proper antecedent basis.

Regarding claim 14, the phrase "on or more" is unclear as to its meaning and relationship to the recited claim elements.

6. The rejections of claims 1-20 using Nishiyama et al and Nishiyama et al in view of Georgiou et al are withdrawn in view of applicant's amendments and arguments that the processor units are entire processors such as RISC processors or DSP processors that can operate stand-alone at page 6 of the amendment.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1 and 9-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Brock et al., U. S. Published Application 2002/0147932.

Per claim 1:

A) Brock et al teach the following claimed items:

1. a plurality of processor units each having a clock input that controls the performance of the unit (Local Set Points 110) with processor units 103, 104, 105 and 106 figure 1, at page 3, paragraphs 25 and 26;

2. a controller having a plurality of clock outputs (Local Controls 203) each coupled to the clock inputs (Local Set Points 110) with Power/Performance Controller 201 of figure 2 and at page 4, paragraph 27;

3. the controller varying the clock frequency of each processing unit to optimize power consumption and processing power for a task with figure 4 and at page 4, paragraphs 27 and 30.

Per claims 9-16:

Brock describes changing a clock rate independently of the remaining processor units at page 3, paragraph 25. Brock describes generating the clock rate based on an algorithm (figure 4) optimized for power reduction or emissions control (EMC and noise levels) based on tasks handled by each processor unit and invoked by external or internal stimuli (parameters 204 through 207 of figure 2) with figures 2 and 4 and at page 4, paragraph 27. Brock describes the controller changing clock inputs on-the fly with element 407 of figure 4. Brock describes controlling clock inputs in a centralized manner with the global controls of figures 2 and 4 and at page 4, paragraph 27. Brock describes controlling clock inputs in a decentralized manner with the local controls of figures 2 and 4 and at page 4, paragraph 27.

9. Claims 2-8 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brock et al., U. S. Published Application 2002/0147932 in view of Nishiyama et al., U. S. Patent 5,790,877.

Per claim 3:

Brock et al teach the elements of claim 1 as described in the above rejection. The claims seem to differ from Brock et al in that Brock et al fails to explicitly teach one of the processor units is a RISC processor as claimed. Nishiyama teaches that it is known to provide a processor unit that is a RISC processor at column 3, lines 35-42. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make at least one of the processor units a RISC processor, as taught by Nishiyama, in order to apply Brock's power and performance control system to processing units having RISC architecture. One of ordinary skill in the art would have been motivated to combine Brock and Nishiyama because of Nishiyama's suggestion that power control systems that control the processor clock frequency are equally applicable to a RISC type processor at column 3, lines 35-42. It would have been obvious for one of ordinary skill in the art to combine Brock and Nishiyama because they are both directed to the problem of reducing the power consumption of processors by individually controlling the clock frequency to each processor unit.

Per claims 4-6 and 18:

Nishiyama describes one of the processing units comprises a RISC processor at column 3, lines 35-42. Nishiyama describes dynamically managing each unit on

a per task basis at column 2, lines 37-65 and at column 6, lines 9-18. Nishiyama describes each unit clocked at the lowest rate possible to reduce peak power dissipation or average dissipation at column 2, lines 52-60 and at column 6, lines 9-18. Nishiyama describes the controller generating a plurality of clock signals with figure 2 and independently controlling the rate to each processing unit at column 3, lines 64-67 and at column 4, lines 21-34. Nishiyama describes the clock rate based on a pre-assigned algorithm optimized for power reduction with the compiler, figures 5 and 6 and at column 4, line 60 – column 5, line 16. Nishiyama describes controlling clock inputs on-the-fly and a centralized controller at column 3, lines 43-67.

Per claims 2, 7-8, 17 and 19-20:

Brock does not explicitly describe one of the processing units comprises a DSP. Brock fails to describe the details of the type of processing units processors 103 through 106 of figure 1 may comprise. However, the examiner has already presented evidence that DSPs are well known and their power consumption may be reduced by reducing the DSP clock frequency. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a controller that outputs a plurality of clock outputs to one or more DSP processing units in order to apply Brock's power and performance system to a processor core having at least one DSP processing unit. Brock describes generating a plurality of clock from a master (reference) clock using PLL circuits at paragraph 26. It would have been obvious to one having ordinary skill in the

art at the time the invention was made to provide gated clocks in order to independently stop transmission of a clock signal to one or more of the processing units. Brock describes controlling the clock frequency based on temperature and other physical parameters with figures 2 and 4. Brock does not describe the details of how the clock frequency is changed. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to allow for arbitrary increments of the clock in order to provide the optimal clock frequency for each processor based on the sensor inputs. Brock does not explicitly describe providing a buffer or FIFO buffer between two processor units. However, Brock describes that communication between processors is accomplished by I/O circuits 111 and 114 of figure 1. Brock describes two processors directly communicating via line 115 using I/O circuits 111 and 114 of figure 1 at paragraph 25. It is well known that I/O circuitry includes buffer circuitry and it would have been obvious for one of ordinary skill in the art to include a FIFO buffer in the I/O circuitry of Brock to allow for communication between the two processors.

10. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Dennis M. Butler

Dennis M. Butler
Primary Examiner
Art Unit 2185